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Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Hirokazu YAMADA
FOR: DATA PROCESSING APPARATUS

Enclosed are:

- ☒ 30 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☒ Certified copies of Japanese Patent Application Nos. 11-258728, 11-258730, 11-258732, and 11-258736
- ☒ 13 sheets of formal drawing.
- ☒ An assignment of the invention to MINOLTA CO., LTD. and the assignment recordation fee.
- ☐ An associate power of attorney.
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- ☒ Information Disclosure Statement, Form PTO-1449 and reference.
- ☒ Return Receipt Postcard
- ☐

The filing fee has been calculated as shown below:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	12	-20	0	$18.00	$0.00
Independent Claims	5	-3	2	$78.00	$156.00
				Multiple Dependent Claim(s)	$0.00
				Basic Fee	$690.00
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Respectfully submitted,

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DATA PROCESSING APPARATUS

This application is based on application Nos. Hei 11-258728, Hei 11-258730, Hei 11-258732 and Hei 11-258736 filed in Japan, the content of which is hereby incorporated by reference.

FIELD OF THE INVENTION

The present invention relates to a processing apparatus for correcting image data and, more particularly, to an apparatus for forming an image by superimposing a plurality of colors based on image data on the plurality of colors.

DESCRIPTION OF THE RELATED ART

In a tandem-type image forming apparatus such as a tandem-type color printer or a tandem-type color copier, recording units (print heads) for the four colors of yellow (Y), magenta (M), cyan (C), and black (K) are arranged in a row. In the image forming apparatus, a plurality of toner images C, M, Y, and K generated by these recording units are superimposed and transferred onto a single sheet to form a color image.

To increase the quality of color printing, misregistration of the transferred toner images in the

plurality of colors should be reduced. The misregistration includes misregistration in the main scanning direction which is perpendicular to the direction of sheet transportation, misregistration in the sub-scanning direction which is the direction of sheet transportation, and misregistration based on the amount of skew of the inclination of a line in the main scanning direction. Misregistration between the print heads is classified into three types, which are misregistration in the main scanning direction, misregistration in the sub-scanning direction, and inclinational misregistration. The misregistrations in the main scanning direction and in the sub-scanning direction can be corrected relatively easily by controlling the timing with which data on the individual colors is outputted from a printer controller. For the inclinational misregistration, however, it becomes necessary to correct image data in accordance with the amount of inclination. For smooth printing of a corrected image, correction should be performed on a unit basis smaller than one pixel.

For the correction of skew produced between the print heads, the inclination can be reduced by disposing a line buffer equivalent to the maximum amount of inclination that requires correction immediately anterior to the print heads and correcting the image data in accordance with the amount of inclination by using the line buffer. However, this

method requires a large quantity of memories operable at a high speed for correction and, if the maximum inclination assumed is exceeded, correction cannot be performed.

SUMMARY Of THE INVENTION

An image forming apparatus according to the present invention is an apparatus for performing image formation in overlapping relation on a single sheet by using a plurality of print heads arranged in a row, the apparatus comprising: first correcting means for correcting image data on a line basis in a sub-scanning direction based on the amount of relative inclination between the print heads; and second correcting means for correcting the image data corrected by the first correcting means on a unit basis smaller than one line.

By performing correction in the two separate operations, it is possible to perform the correction on a 1-line basis in an image memory and perform the correction on a unit basis smaller than one line in a FIFO memory or a print head portion. This reduces the quantity of special memories required for correction, such as FIFO memories, and achieves lower cost.

In the image forming apparatus, the amount of inclination is detected as an integral multiple of a unit for correction in the correction performed by the second

correcting means on a unit basis smaller than one line.

This simplifies the structure of the second correcting means and enables a high-accuracy correcting process.

An image forming apparatus according to the present invention is an apparatus for performing image formation in overlapping relation on a single sheet by using a plurality of print heads arranged in a row, the apparatus comprising: a bit map memory having an image data region for storing image data and respective blank regions provided on leading and rear end portions of the image data region; a read address generating unit for sequentially generating read addresses from a leading address in the image data region of the bitmap memory; a write address generating unit for generating, from the read addresses, write addresses by correcting relative inclination between the print heads on a line basis; and a memory control unit for reading, from the read addresses generated by the read address generating unit, image data stored in the image region of the bitmap memory and writing the image data at the write addresses generated by the write address generating unit. Preferably, the dimensions of the blank regions is equal to or larger than the maximum amount of inclination to be corrected.

Since the respective blank regions (white data regions) are provided on the leading and rear end portions

of the image data, the memory control unit can perform correction on a line basis by transferring the image data in the bitmap memory. By transmitting, to the print heads, the image data that has been corrected preliminarily against the relative inclination between the print heads, the inclination can be cancelled out.

An image forming apparatus according to the present invention is an apparatus for performing image formation in overlapping relation on a single sheet by using a plurality of print heads arranged in a row, the apparatus comprising: a bitmap memory having an image data region for storing image data and specified blank regions provided on leading and rear end portions of the image data region, respectively; a read address generating unit for generating read addresses for image data based on correction data on relative inclination between the print heads; and an output unit for reading the image data from the generated read addresses.

In the arrangement, the apparatus outputs the image data in the bitmap memory at a high speed, while performing a correcting process with respect thereto, in correcting skew produced between the print heads.

Since the apparatus outputs the image data in the bitmap, while performing the correction on a line basis, the correction can be performed on a unit basis equal to or

smaller than one line in a buffer memory having a capacity of at least one line of data.

An image forming apparatus according to the present invention is an apparatus for image formation in overlapping relation on a single sheet by using a plurality of print heads arranged in a row, the apparatus comprising: a bitmap memory for storing image data; a read address generating unit for consecutively generating read addresses for image data based on relative inclination between the print heads on the unit basis of one burst access; and a memory control unit for reading the image data from the bitmap memory at the read addresses generated by the read address generating unit.

The apparatus further comprises storing means for temporarily storing the read image data, the storing means having a capacity of at least one line of data, wherein the memory control unit comprises a selecting unit for selectively outputting either of the image data read from the bitmap memory and the image data stored in the storing means based on the relative inclination between the print heads.

The apparatus further comprises storing means for temporarily storing the read image data, the storing means having a capacity of at least one line of data and storing, of the data read by a burst access from the addresses

generated by the read address generating unit, data of the length of a specified unit for correction.

These and other objects, advantages and features of the invention will become apparent from the following description thereof taken in conjunction with the accompanying drawings which illustrate specific embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

In the following description, like parts are designated by like reference numbers throughout the several drawings.

Fig. 1 is a cross-sectional view of the overall structure of a color printer;

Fig. 2 is a block diagram of an image data control unit;

Fig. 3 is a view for illustrating the concept of skew correction;

Fig. 4 is a view showing the procedure of skew correction;

Fig. 5 is a view showing an example of skew correction;

Figs. 6A, 6B, 6C and 6D are views for illustrating skew correction in a memory;

Fig. 7 is a block diagram of an address generating

circuit;

Figs. 8A, 8B, 8C and 8D are views for illustrating skew correction in reading data from the memory;

Fig. 9 is a timing chart of a conventional access;

Fig. 10 is a timing chart of a burst access;

Fig. 11 is a 1-line-based correcting circuit diagram;

Fig. 12 is a timing chart of correction by the burst access;

Fig. 13 is a block diagram of an address generating circuit;

Fig. 14 is a block diagram of a select signal generating circuit;

Fig. 15 is a timing chart of the select signal generating circuit;

Fig. 16 is a 1/3-line-based correcting circuit diagram;

Fig. 17 is a block diagram of the select signal generating circuit;

Fig. 18 is a timing chart of the select signal generating circuit;

Fig. 19 is a view showing a structure of a print head portion; and

Fig. 20 is timing chart of the print head portion.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the accompanying drawings, the embodiments of the present invention will be described. In the drawings, the same reference numerals designate identical or equivalent components.

Fig. 1 shows a schematic structure of a tandem-type color printer to which the present invention has been applied. Imaging units 10y, 10m, 10c, and 10k for the four colors of yellow (Y), magenta (M), cyan (C), and black (K) are successively arranged in a row in the direction (sub-scanning direction) in which a sheet on a transfer belt 12 moves. In each of the imaging units 10y, 10m, 10c, and 10k, elements necessary to perform an electrophotographic process are disposed around a photosensitive member having a rotation axis disposed in the main scanning direction. With the photosensitive members for Y, M, C, and K image formation rotating counterclockwise in the drawing, an image formation process is performed continually in the imaging units 10y, 10m, 10c, and 10k. Image data transmitted from a host is converted into individual sets of data for printing in yellow, magenta, cyan, and black in a control unit 14, which are transmitted to respective exposing heads in the imaging units 10y, 10m, 10c, and 10k. Each of the exposing heads emits laser light in response to an electric signal of the transmitted set of image data, scans the photosensitive member with the light in the main

scanning direction by using a polygon mirror, and thereby exposes the photosensitive member. Latent images formed on the photosensitive members are developed with toners in the individual colors. The toner images on the photosensitive members are transferred in overlapping relation to the transfer belt 12 by a transfer charge (not shown) disposed in the transfer belt 12 in opposing relation to each of the photosensitive members. On the other hand, the sheet is transmitted from a sheet feeding cassette 16 by a pickup roller 18. The toner images on the transfer belt 12 are transferred onto the sheet by the transfer roller 20. The toner images are melted with the application of heat and fixed onto the sheet by a fixing unit 22 and then discharged into a tray 25 via a sheet transport path 24. The toners remaining on the transfer belt 12 after the transfer are removed by a cleaner 26.

Most downstream of the imaging units 10y, 10m, 10c, and 10k, three resist correction sensors 28 are arranged in a row in a direction (in the main scanning direction) perpendicular to the direction of transport of the belt 12. When a resist pattern is formed on the transfer belt 12 by using the imaging units 10y, 10m, 10c, and 10k, the sensors detect the amount of color misregistration of the Y, M, C, and K toner images in the main and sub-scanning directions such that the image data control unit corrects an image

forming position and image distortion. This prevents color misregistration of the Y, M, C, and K toner images on the sheet.

In the control unit 14 shown in Fig. 2, a CPU 30 controls the operation of the whole control unit. To the CPU 30, a ROM 32 and a DRAM 34 are connected. On the other hand, a memory-I/O control unit 36 controls a memory and signal inputting and outputting from and to the outside. The CPU 30 is also connected to a host interface unit 38, a video interface unit 40, and a skew correction control unit 42. Image data is stored in the DRAM 34 via the host interface unit 38. The skew correction control unit 42 controls skew correction by using a line buffer 44.

Next, a description will be given to skew correction. Fig. 3 shows an example of skew between the print heads in the imaging units 10y, 10m, 10c, and 10k. Here, respective skew distortions of yellow, magenta, and cyan are presented relative to the line in black (K) as a reference. The skew distortions are due to the inclinations of the print heads or the like and detected by the resist correction sensors 28.

Fig. 4 shows the outline of a correcting procedure by the skew correction control unit 42. A first skew correcting portion 42a performs rough skew correction on a 1-line basis for mechanical variations of the print heads

with respect in the image data in an image memory (DRAM 34). Next, a second skew correcting portion 42b performs skew correction on a unit basis smaller than one line with respect to the data corrected by the first skew correcting portion. In the present embodiment, it is assumed that printing can be controlled on a 1/3-dot basis in the sub-scanning direction. In the case of performing skew correction on a 1/3-line basis, therefore, the second skew correcting portion 42b uses appropriately correction data of 3n (n is a natural number), which is an integral multiple of the divisor. In this case, the amount of 1-line-based correction can be adjusted to n and processing can be performed with a simple circuit. Specifically, if the correction data on a 1/3-line basis is assumed to be 3n+1 or 3n+2, a fraction is produced so that an additional circuit for processing the fraction becomes necessary. If the correction data is assumed to be 3n, correctable accuracy is reduced to 1/3 but the processing of the fraction described above becomes unnecessary and the circuit can be simplified. Obtained image data is transmitted to the print heads. By thus performing correction in the two separate operations, it is possible to perform, e.g., the correction on a 1-line basis in the image memory and the correction on a unit basis smaller than one line in a FIFO memory or in the print head. This

reduces the quantity of special memories required for correction, such as FIFO memories, and achieves lower cost.

It is assumed here that the line formed by the yellow, magenta, or cyan print head is inclined relative to the black line as the reference and a skew distortion has been caused thereby, as shown in the upper portion of Fig. 5. Here, the solid circle represents one dot. As shown in the middle portion of Fig. 5, the first skew correcting portion 42a performs the 1-line-based correction. As subsequently shown in the lower portion of Fig. 5, the second skew correcting portion 42b performs the 1/3-line-based correction. By effecting printing by using data after correction, the skew distortion can be reduced to a degree smaller than one line.

In the present embodiment, the 1-line-based skew correction is performed by processing, in the memory, image data stored in the bitmap memory region within the DRAM 34. By transmitting, to the print head, image data that has been previously corrected against the skew distortion, the skew distortion can be cancelled out.

Figs. 6A, 6B, 6C and 6D are representations of image data in a two-dimensional space in skew correction. A description will be given to the correction within the memory with reference to Figs. 6. As shown in Fig. 6A, respective white data regions are provided in the leading

end portion (upper portion in the drawing) 52 of the image data (before correction) 50 received from the host and in the rear end portion (lower portion in the drawing) 52 thereof in the bitmap memory. The white data regions have dimensions equal to or larger than the maximum amount of inclination to be corrected.

In the skew correction, the first line of the image data 50 before correction is initially transferred to the upper white region 52 by using the line buffer 44, as shown in Fig. 6B. The position to which the first line is transferred becomes oblique in response to the skew distortion detected by the resist correction sensors 28. Here, the image data in the uppermost portion is transferred to the position in contact with the uppermost portion of the white region 52. Likewise, data on the second and subsequent lines is transferred sequentially to the positions subsequent to the data on the first line, as shown in Fig. 6C. Fig. 6D shows image data after the completion of the transfer. Since data in the white region 54 is similarly transferred, white data is stored automatically in a lower portion of the image data where the image data no more exists. Thus, the white region on the lower side of the image is expanded to the upper side, which obviates the necessity for the process of removing data in the portion of the bitmap memory where the image

data does not exist during data transfer or after data transfer.

Fig. 7 shows an address generating circuit when skew correction is performed within the memory 34, as shown in Figs. 6A-6D. The address generating circuit is in the skew correction control unit 42. In the address generating circuit, an address counter 60 counts in response to an image clock by using a start address stored in a start address register 62 as an initial value. In a read operation, if an image clock signal is inputted, the address counter 60 increments the count value by 1 and outputs the incremented count value as a read address. In a write operation, the count value in the address counter 60 and an offset value stored in an offset register 64 are added up by a first adder 66 and outputted to a second adder 68. If a pixel clock signal is inputted, on the other hand, a skew counter 70 receives, in response to a line synchronizing signal, a skew correction value stored in a skew correction value register 72 and counts by using the skew correction value as an initial value. A multiplier 74 calculates the product of the count value in the skew counter 70 and a value in a main scanning register 76 and outputs the calculated product as a value obtained by skew correction to the second adder 68. The second adder 68 adds up the two input values and outputs the sum

as a write address.

In another embodiment, correction is performed while image data in the bitmap memory is outputted at a high speed in line-based skew correction. If a description is given with reference to Figs. 8A, 8B, 8C and 8D, respective white data regions are provided in the upper and lower portions of image data received from the host in a two-dimensional space, as shown in Fig. 8A. The white data regions have dimensions equal to or larger than the maximum amount of inclination to be corrected (this is the same as in the case of the first embodiment shown in Figs. 6A-6D). In skew correction, the address generating circuit (see Fig. 13) generates a read address the position of which is represented by oblique lines in response to correction data on a skew distortion. That is, in the two dimensional space, image data stored as shown in Fig. 8A is read obliquely so as to cancel out the skew distortion. First, as shown in Fig. 8B, the first line of the image data is read as video data at a read position represented by the oblique lines. Of the first line, only the data of the final 1/4 part is image data. Data of the second and subsequent lines is similarly transferred to the positions subsequent to the first line, as shown in Fig. 8C. Fig. 8D shows the final reading of the final line of the image data. Of the final line, only the data of the initial 1/4 part is

image data.

Next, a description will be given to a burst access mode. Conventionally, image data has been read out of predetermined addresses on a 1-word basis, as shown in, e.g., the access timing chart of Fig. 9. Here, an access to data for 4 words is shown. By contrast, the present embodiment reads image data by a burst access. In the burst access, if a leading address is specified, data for a plurality of words (here, 4 words) is accessed collectively. Fig. 10 shows the timing for the burst access. In line-based correction, image data is read on the basis of the plurality of words by the burst access. Accordingly, 4 sets of data are read consecutively by generating an address at which data is read from the bitmap memory on the basis of one burst access. That is, if the address is outputted, data at four addresses including the address is accessed consecutively. Since the reading of the image data is performed by the burst access, it will be understood by comparison with Fig. 9 that an access time can be reduced and a correcting process can be performed at a higher speed.

Next, a description will be given to the 1-line-based correcting circuit 42a with reference to Fig. 11. Addresses for one line of data are outputted sequentially from an address generating circuit (see Fig. 13) 80 to the

image memory 34 by a burst access. The output data from the image memory 34 is transmitted directly to a selector 84, while it is also transmitted to the selector 84 via the line buffer 44. The selector 84 synthesizes, on a pixel basis, one line of image data from two lines of data in response to a select signal from a select signal generating circuit 86 (see Fig. 14) and outputs the synthesized data.

Referring to Fig. 12, a description will be given to skew correction using the bust access performed in the 1-line-based correcting circuit 42a. For the skew correction, data before correction is read on a word basis in a two dimensional space. The unit for skew correction based on the inclination of the print heads (hereinafter referred to as a correction unit) is not necessarily an integral multiple of a unit in which data is read by one burst access (hereinafter referred to as an access unit). In the upper stage of Fig. 12, it is shown that, for the data before correction, data read by the n-th, (n+1)-th, and (n+2)-th burst accesses is in overlapping relation. If data is read in the access unit, therefore, unwanted data shown in the hatched portions is also read. It follows that necessary data in overlapping relation to the unwanted data cannot be read. Therefore, correction is performed by using the 1-line line buffer (FIFO memory) 44 as shown in the middle stage of Fig. 11. In the example shown in the

drawing, the portions of data in the three correction units that have been already shown in hollow portions are stored in the line buffer 44, as indicated by the arrows. Although the hatched portions are read by the burst accesses, they are not included in the correction units so that they represent the portions not stored in the line buffer 44. When image data is newly read by the subsequent access, data that has not be read by the previous access (the hollow portions) is synthesized at the corresponding position of the line, as indicated by the arrows, while it is also stored in the line buffer 44 simultaneously. Thus, as shown in the lower stage of Fig. 12, one line of data is synthesized on a pixel basis from two lines of data.

Fig. 13 is a block diagram of an address generating circuit 80 based on the burst access. An image clock is inputted to a dot counter 800 and a frequency divider 802. The frequency divider 802 divides the frequency of the image clock into units in which the burst access is made (access unit) and transmits it to an address counter 804. The address counter 804 is incremeneted based on the access unit by using a start address inputted from a start address register 806 as an initial value and outputs the address to an adder 808.

On the other hand, the dot counter 800 outputs a count pulse to a line counter 812 every time the unit of

pixels to be corrected, which is stored in a skew correction value counter 810, is reached. The output value from the line counter 812 and the line size from a line size register 814 are added up by an adder 816 and the sum is outputted to an adder 818. As a consequence, the multiplier 816 calculates the number of lines to be corrected. The dot counter 800 and the line counter 812 are reset by the line synchronizing signal. The adder 818 adds up the two input values and outputs a read address.

Fig. 14 is a block diagram of a select signal generating circuit 86 and Fig. 15 is a timing chart thereof. A word counter 860 and a skew counter 862 are repeat counters for counting pixel clocks. The word counter 860 is reset every time the unit for burst access (access unit), which is stored in a word register 864, is reached and the skew counter 862 is reset every time the unit of pixels to be corrected, which is stored in a skew register 866, is reached. The skew register 866 resets the skew counter 862 by outputting the value stored therein in response to an output signal from the skew counter 862 or to the line synchronizing signal. The word register 862 resets the word counter 860 by outputting the value stored therein in response to an output signal from the word counter 860 or to the line synchronizing signal. A flip-flop 868 is reset in response to the output signal from the skew counter 862

and set in response to the output signal from the word counter 864 to output a select signal. When the select signal is set, data from the line buffer 44 is selected. When the select signal is reset, data from the image memory 34 is selected.

As described above, the respective white data regions are provided in the leading and rear end portions of the image data in the bitmap memory (see the upper left portion (a) of Figs. 8) and image data is outputted, while line-based correction is made by using the line buffer 44. Thus, the 1-line-based correction can be performed by using the line buffer 44 having a capacity of at least one line of data. This reduces the quantity of special memories required for skew correction, such as FIFO memories, and achieves lower cost.

For smooth printing of an image, the correction should be performed on a unit basis smaller than one pixel. Next, a description will be given to the correction performed by the second skew correcting portion 42b on a unit basis smaller than one line (in the present embodiment, on a 1/3 line basis). As shown in Fig. 4, the correction on a unit basis smaller than one line is made with respect to image data that has been corrected on a 1-line basis by the first skew correcting portion 42a. In the correction performed on a unit basis smaller than one line, printing

is controlled on a 1/3-line basis in the sub-scanning direction, as shown in Fig. 5.

Fig. 16 shows the 1/3-line-based correcting circuit 42b and a print head 46. Video data that has been already corrected on a 1-line basis is delayed via a line buffer 90. The video data or the video data delayed by one line is outputted as a video 0 signal, a video 1 signal, and a video 2 signal to the print head 46 (see Fig. 19). The video 0 signal, the video 1 signal, and the video 2 signal represent printing data to be printed sequentially on a 1/3-line basis. The video 0 signal represents the video data delayed via the line buffer 90. On the other hand, the vide data and output data from the line buffer are outputted to a first selector 92 and a second selector 94, respectively. The first selector 92 and the second selector 94 output, as a video 1 signal and a video 2 signal, video data selected in consideration of the skew in response to a select 1 signal and a select 2 signal from a select signal generating circuit 96 (see Fig. 17) to the print head 46.

Fig. 17 shows a structure of the select signal generating circuit 96. Fig. 18 shows a timing chart of the select signal generating circuit 96. In the select signal generating circuit 96, a sub-dot counter 960 and a skew counter 962 count image clocks. The sub-dot counter 960 is

reset every time the numeric value stored in a sub-dot register 964 is reached. On the other hand, the skew counter 962 is reset every time the numeric value stored in a skew register 966 is reached. The skew register 966 outputs the value stored therein in response to an output signal from the skew counter 962 or to the line synchronizing signal, while the sub-dot register 964 outputs the value stored therein in response to an output signal from the sub-dot counter 960 or to the line synchronizing signal. A shift register 968 is reset in response to the output signal from the skew counter 962 and shifts an input signal on the H level to output the select 1 signal and the select 2 signal in response to the output signal from the sub-dot counter 960.

As shown in Fig. 18, the sub-dot counter 960 and the skew counter 962 are reset in response to the line synchronizing signal to initiate counting and output a shift clock signal and a clear signal, respectively. In response to these, the shift register 968 outputs the select 1 signal and the select 2 signal. As a consequence, the first elector 92 outputs the video 1 signal to the print head 46 upon receipt of the select 1 signal, while the second selector 94 outputs the video 2 signal to the print head 46 upon receipt of the select 2 signal.

Fig. 19 shows a structure of the print head 46. In

the timing chart of the print head 46 of Fig. 20, the chart on the lower side (b) is an enlargement of the broken line portion of the chart on the upper side (a). A print head 46 comprises an array 100 of LEDs arranged in a row in the main scanning direction. The video 0 signal, the video 1 signal, and the video 2 signal from the second skew correcting portion 42b (Fig. 16) are inputted to three shift registers 102, respectively, and shifted in the line direction by using the image clock as a shift clock. Image data (video 0 signal, video 1 signal, and video 2 signal) in the individual cells of the 3-line shift registers 102 are latched by a three-stage shift register 104 in response to the line synchronizing signal. The video 0 signal, the video 1 signal, and the video 2 signal in the three-stage shift register 104 are shifted with a three-step timing in a direction orthogonal to the shift direction of the shift register 102 in response to a 1/3-line synchronizing signal and outputted to the individual LEDs of the LED array 100.

Although preferred embodiment of the invention have been described in the foregoing detailed description and illustrated in the accompanying drawings, it will be understood that the invention is not limited to the embodiment disclosed, but is capable of numerous rearrangements, modifications and substitutions of parts and elements without departing from the spirit of the

invention. Accordingly, the present invention is intended to encompass such rearrangements, modification and substitutions of parts and elements as fall within the spirit and scope of the invention.

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What is claimed is:

1. An image forming apparatus comprising:

a plurality of print heads arranged in a row;

first correcting means which correct image data on a line basis in a sub-scanning direction based on the amount of relative inclination between the print heads; and

second correcting means which correct the image data corrected by the first correcting means on a unit basis smaller than one line.

2. The apparatus according to claim 1, wherein the first correcting means perform the correction in an image memory and second correcting means perform the correction in a FIFO memory.

3. The apparatus according to claim 1, wherein the first correcting means perform the correction in an image memory and second correcting means perform the correction in a print head portion.

4. The apparatus according to claim 1, wherein the amount of inclination is detected as an integral multiple of a unit for correction in the correction performed by the second correcting means on a unit basis smaller than one line.

5. An image forming apparatus comprising:

a plurality of print heads arranged in a row;

a bit map memory;

a read address generator which sequentially generates read addresses from a leading address in the image data region of the bitmap memory;

a write address generator for generating, from the read addresses, write addresses by correcting relative inclination between the print heads on a line basis; and

a memory controller which writes image data to an image data region of the bitmap memory, wherein the leading and rear end portions of the image data region provide respective blank regions, reads from the read addresses generated by the read address generator, image data stored in the image region and writes the image data at the write addresses generated by the write address generator.

6. The apparatus according to claim 5, wherein the dimensions of the blank regions is equal to or larger than the maximum amount of inclination to be corrected.

7. An image forming apparatus comprising:

a bitmap memory having an image data region for storing image data and specified blank regions provided on leading and rear end portions of the image data region;

a read address generating unit for generating read addresses for image data based on correction data on relative inclination between the print heads; and

an output unit for reading the image data from the generated read addresses.

8. An image forming apparatus comprising:

a plurality of print heads arranged in a row;

a bitmap memory for storing image data;

a read address generator for consecutively generating read addresses for image data based on relative inclination between the print heads on the unit basis of one burst access; and

a memory controller for reading the image data from the bitmap memory at the read addresses generated by the read address generator.

9. The apparatus according to claim 8, further comprising storing means for temporarily storing the read image data, the storing means having a capacity of at least one line of data, wherein the memory controller comprises a selecting unit for selectively outputting either of the image data read from the bitmap memory and the image data stored in the storing means based on the relative inclination between the print heads.

10. The apparatus according to claim 8, further comprising storing means for temporarily storing the read image data, the storing means having a capacity of at least one line of data and storing, of the data read by a burst access from the addresses generated by the read address generating unit, data of the length of a specified unit for correction.

11. A data processing apparatus comprising:

a memory which stores image data;

first correcting means which correct image data on a line basis; and

second correcting means which correct the image data corrected by the first correcting means on a unit basis smaller than one line.

12. The apparatus according to claim 11, wherein said first correcting means includes a read address generator which sequentially generates read addresses from a leading address in the image data region of a bitmap memory, a write address generator for generating, from the read addresses, write addresses by correcting relative inclination on a line basis and a memory controller which writes image data to an image data region of the bitmap memory, wherein the leading and rear end portions of the image data region provide respective blank regions, reads from the read addresses generated by the read address generator, image data stored in the image region and writes the image data at the write addresses generated by the write address generator.

Abstract

An apparatus for performing image formation in overlapping relation on a single sheet by using a plurality of print heads arranged in a row, wherein the apparatus has a first correction portion for correcting image data on one line basis in a sub-scanning direction based on the amount of relative inclination between the print heads; and a second correction portion for correcting the image data corrected by the first correction portion on a unit basis smaller than one line.

Fig.1

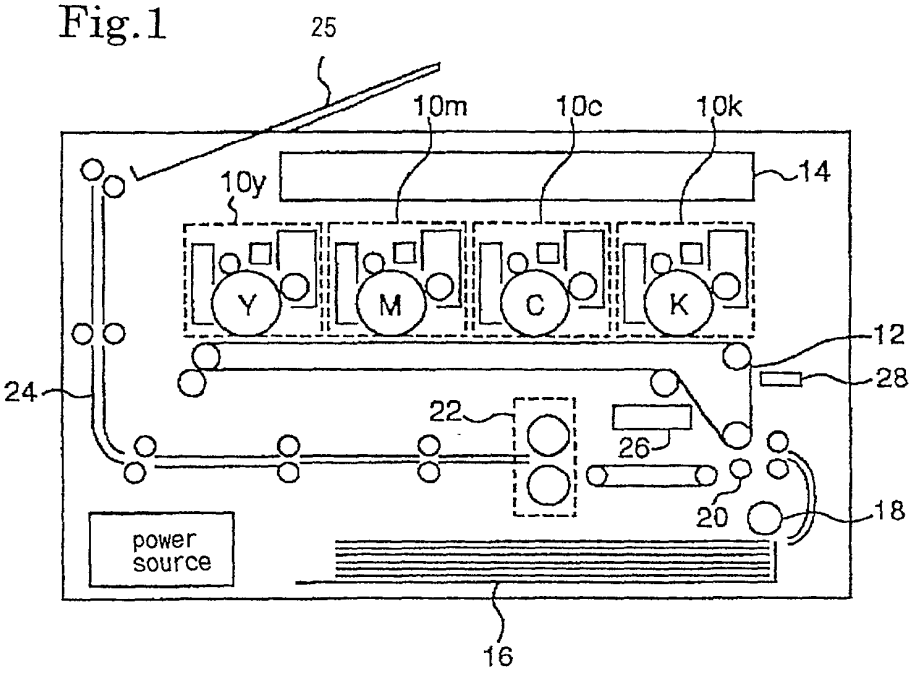

25
10m
10c
10k
10y
14
Y
M
C
K
12
28
24
22
26
20
18
power source
16

Fig.2

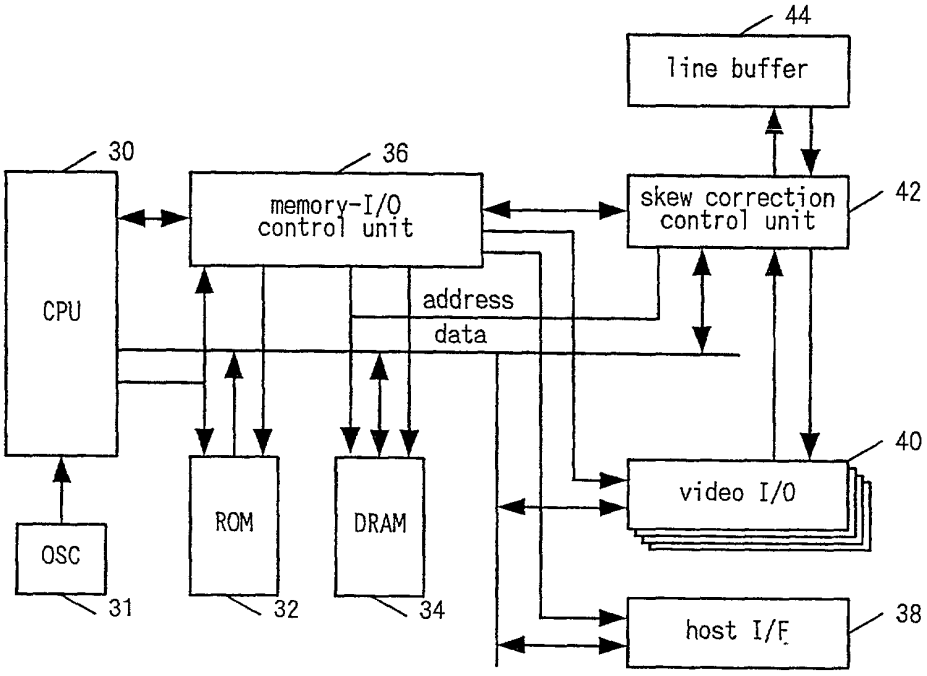

44
line buffer
30
36
memory-I/O control unit
skew correction control unit
42
CPU
address
data
40
video I/O
ROM
DRAM
OSC
31
32
34
host I/F
38

Fig.3

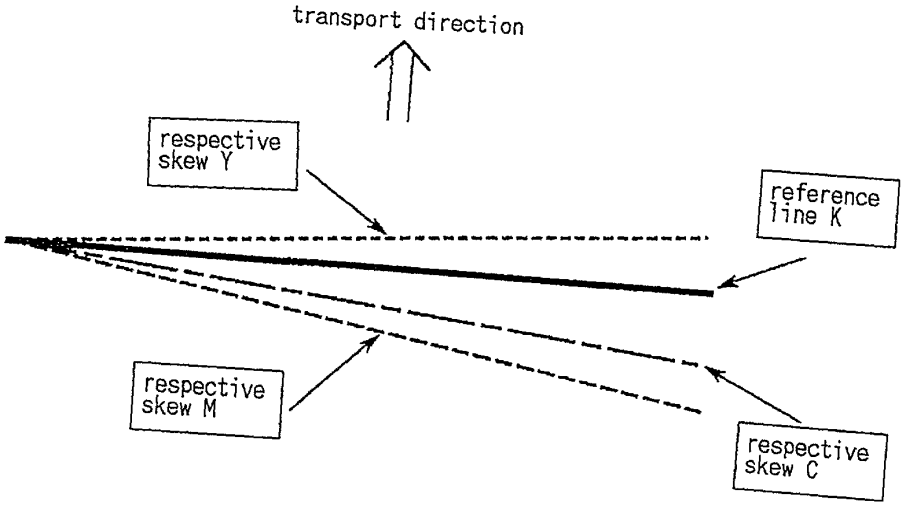

transport direction
respective skew Y
reference line K
respective skew M
respective skew C

Fig.4

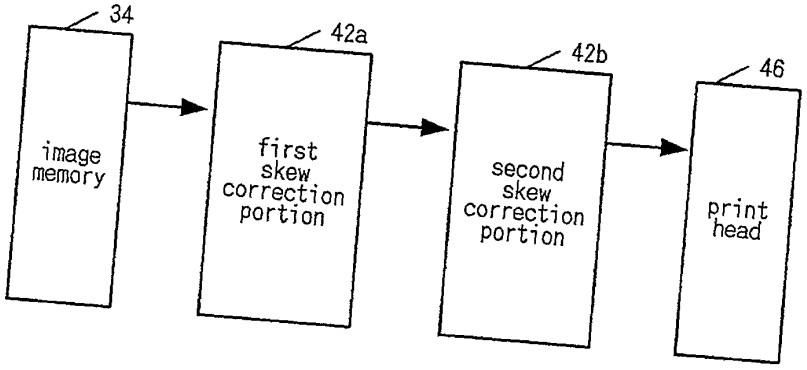

34
image memory
42a
first skew correction portion
42b
second skew correction portion
46
print head

Fig.5

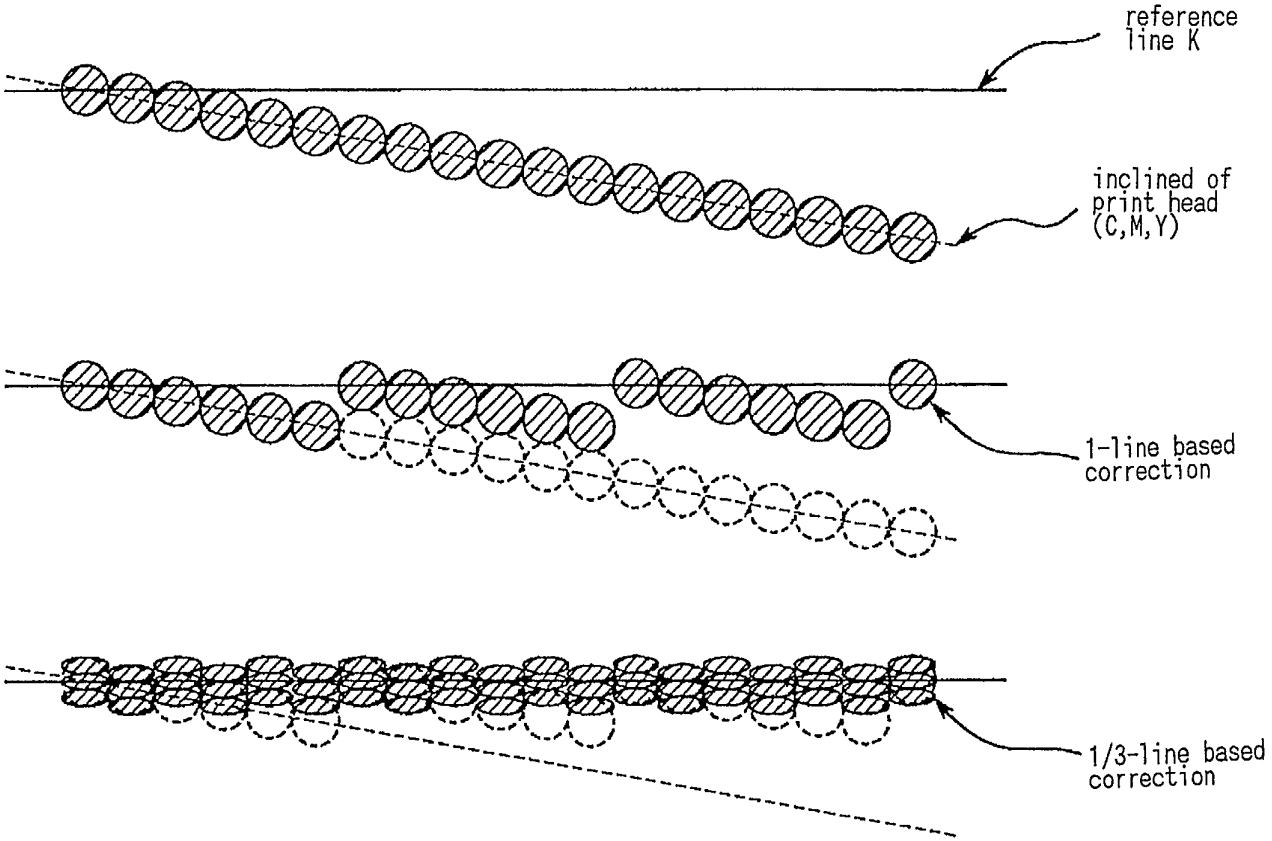

reference line K
inclined of print head (C,M,Y)
1-line based correction
1/3-line based correction

Fig.6A

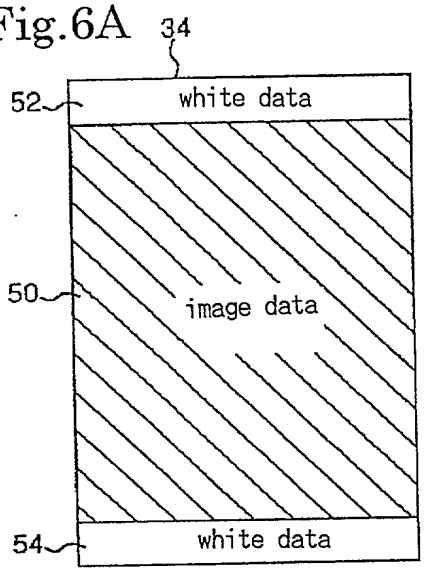


Fig.6B

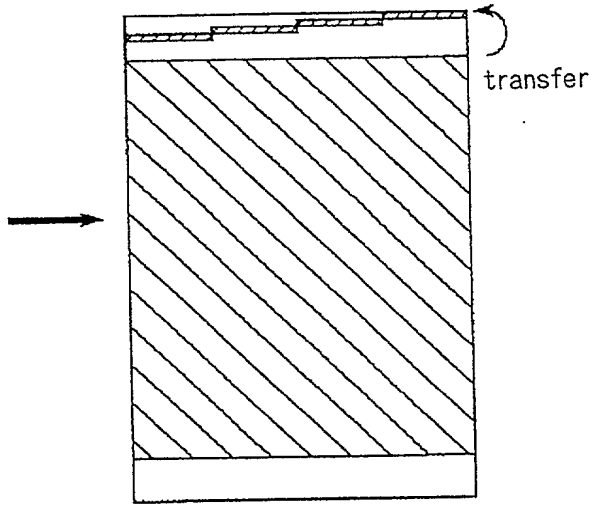


Fig.6C

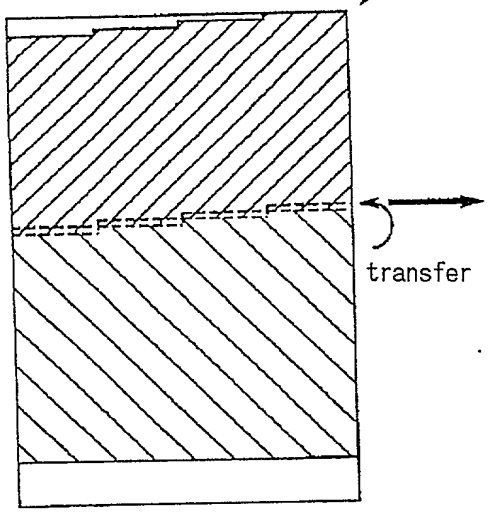


Fig.6D

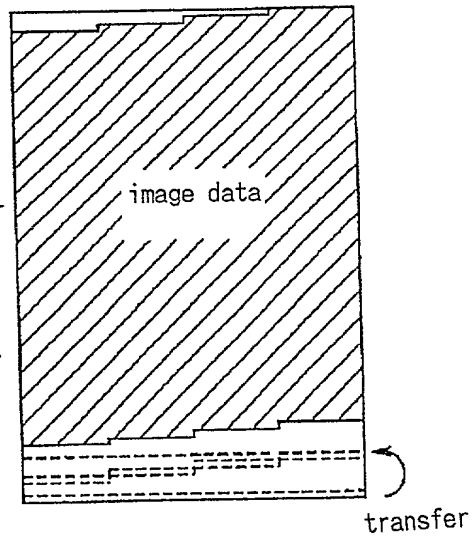


Fig.7

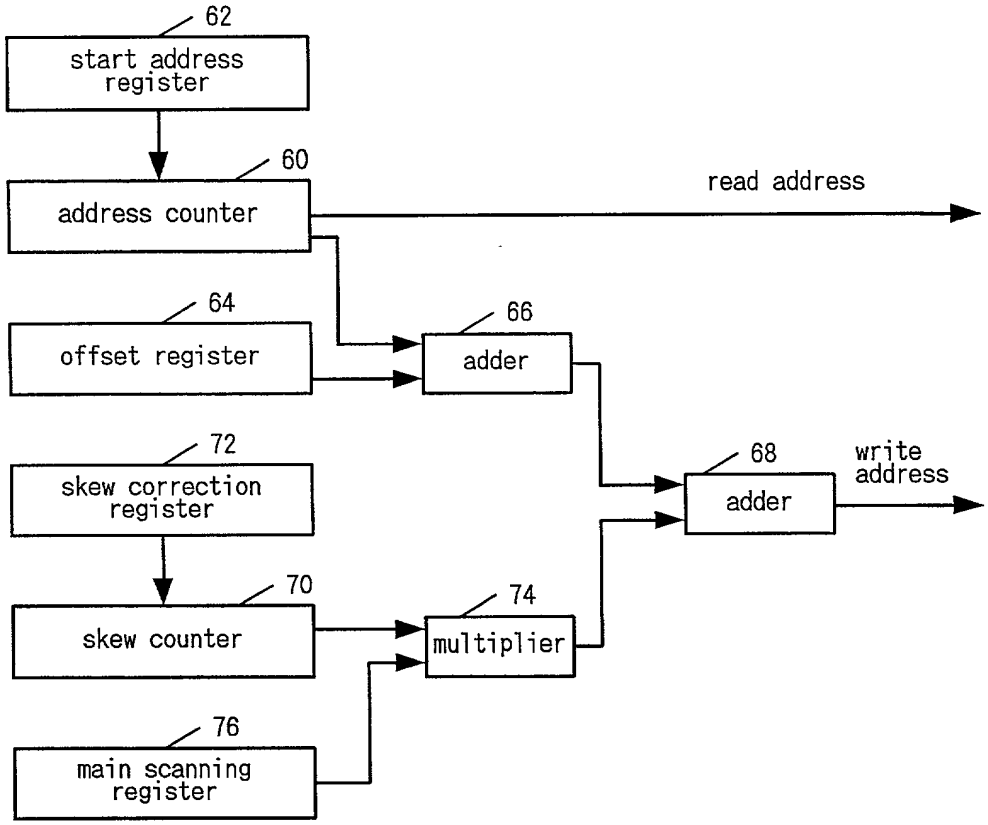

62
start address register
60
address counter
read address
64
offset register
66
adder
72
skew correction register
68
write address
adder
70
skew counter
74
multiplier
76
main scanning register

Fig.8A

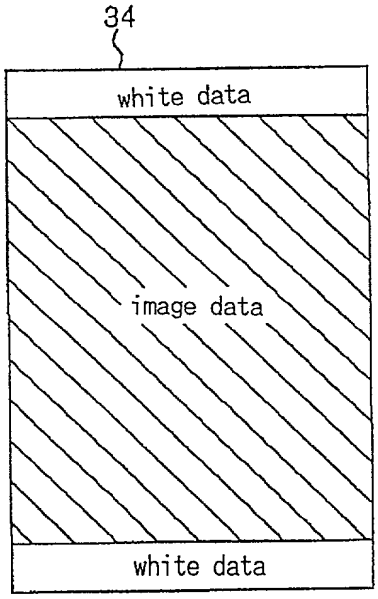


Fig.8B

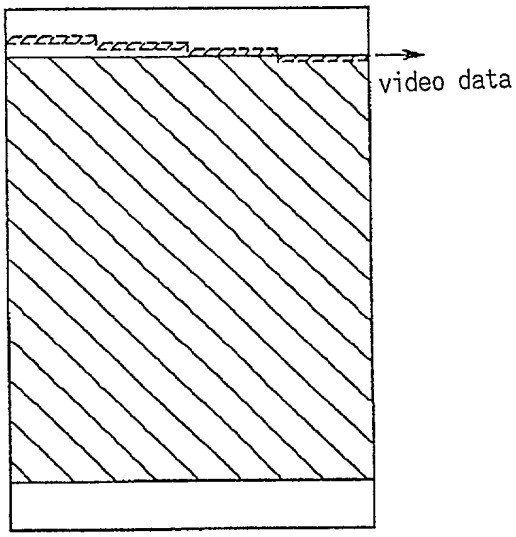


Fig.8C

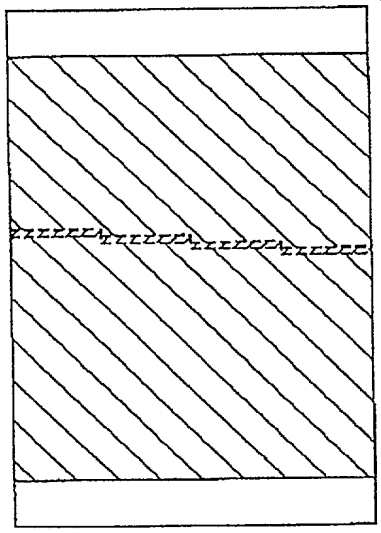


Fig.8D

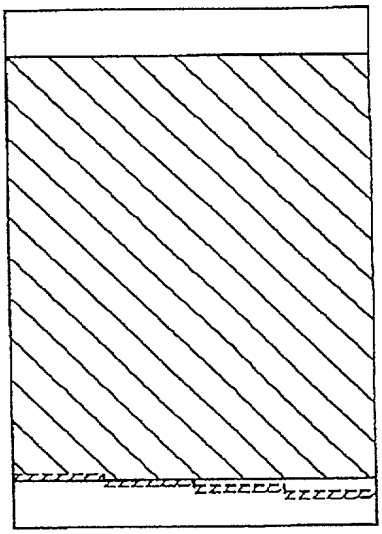


Fig.9

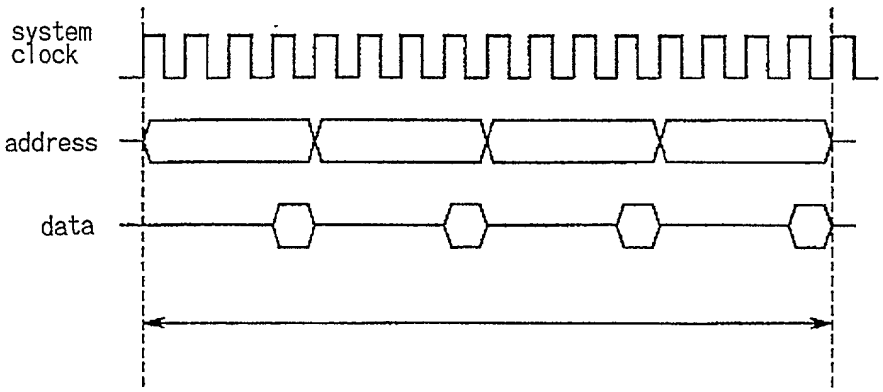


Fig.10

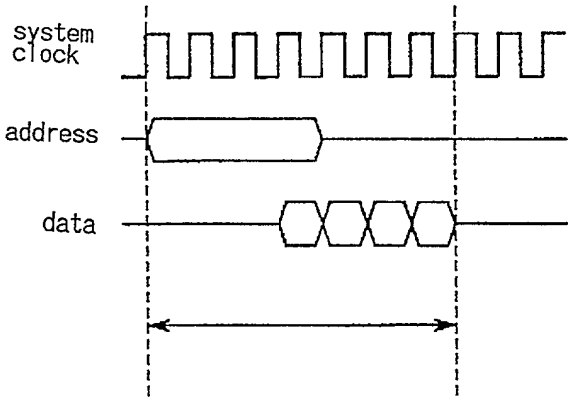


Fig. 11

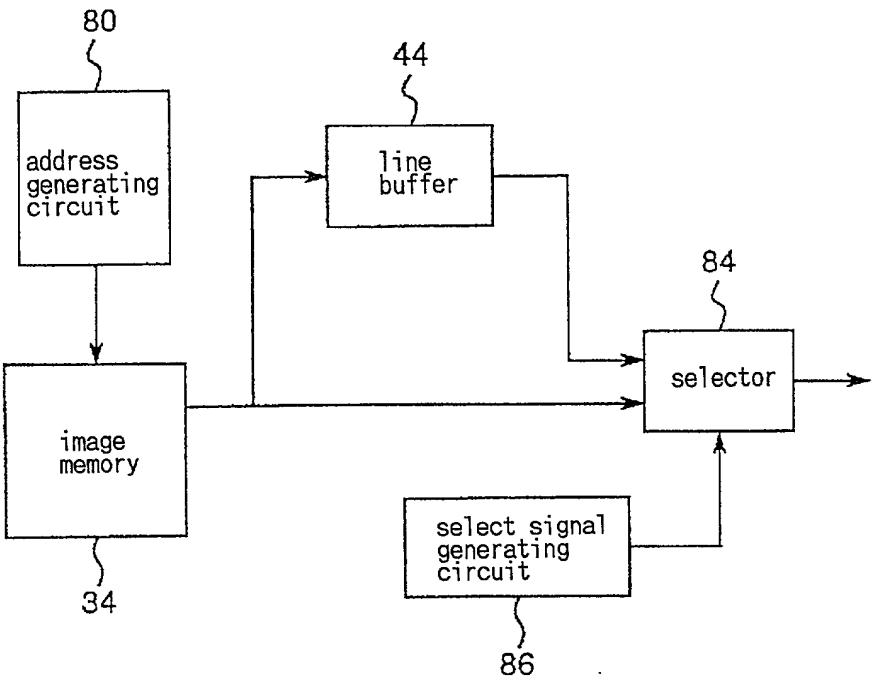

80
address generating circuit
44
line buffer
84
selector
image memory
34
select signal generating circuit
86

Fig.12

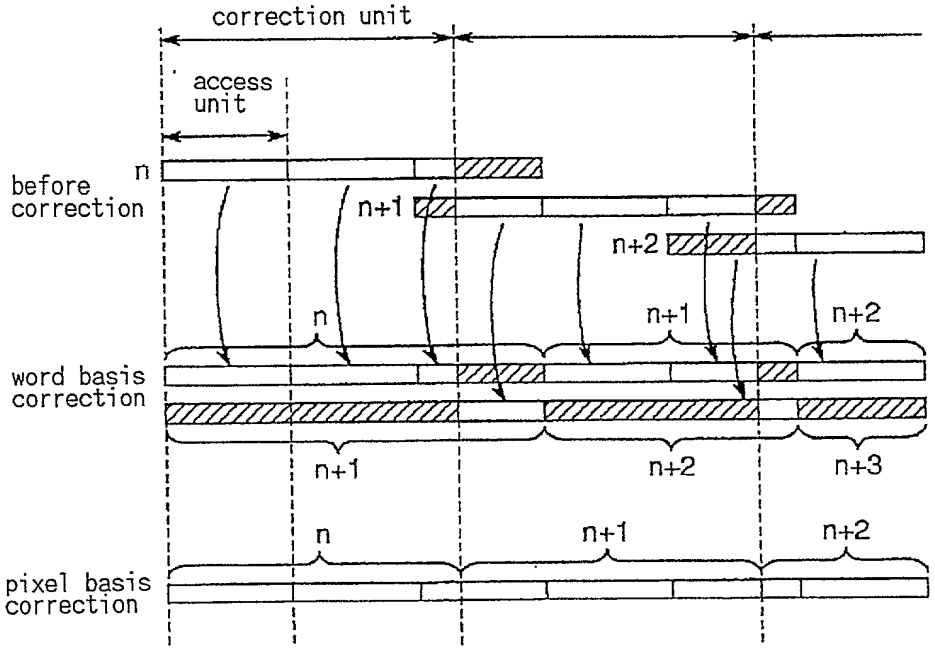

correction unit
access unit
before correction
n
n+1
n+2
word basis correction
n
n+1
n+2
n+1
n+2
n+3
pixel basis correction
n
n+1
n+2

Fig.13

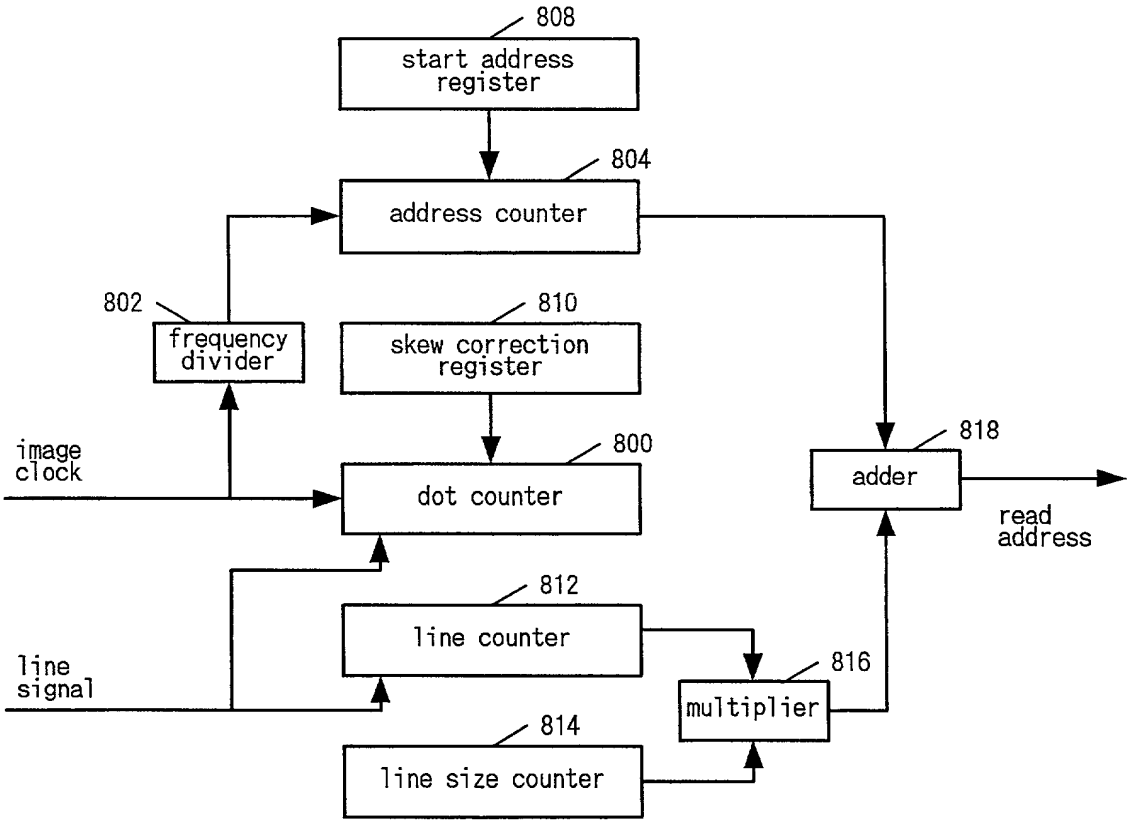

808
start address register
804
address counter
802
frequency divider
810
skew correction register
image clock
800
dot counter
818
adder
read address
812
line counter
line signal
816
multiplier
814
line size counter

Fig.14

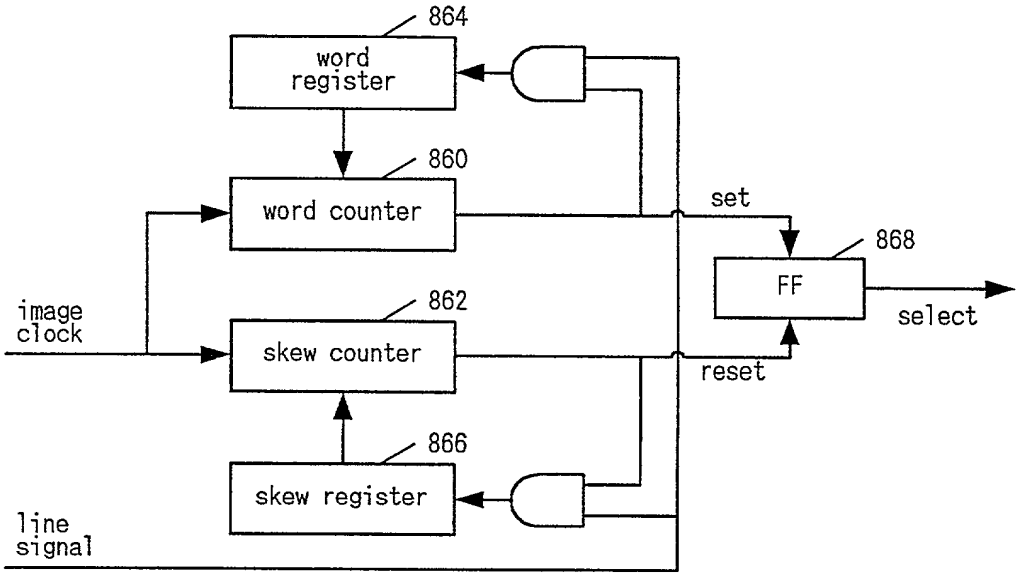

864
word register
860
word counter
set
868
FF
select
image clock
862
skew counter
reset
866
skew register
line signal

Fig.15

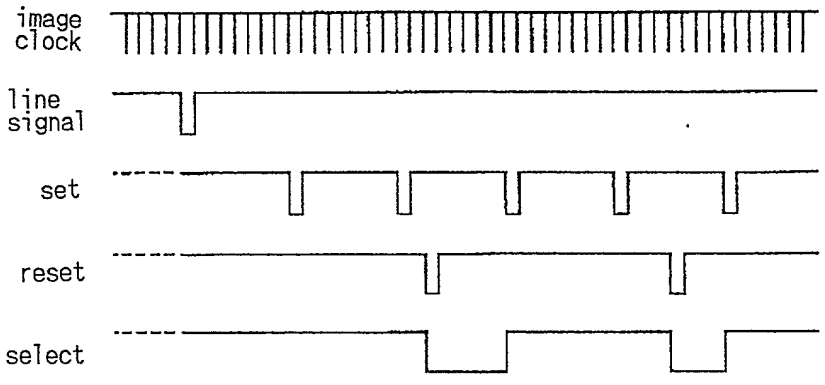


image clock
line signal
set
reset
select

Fig. 16

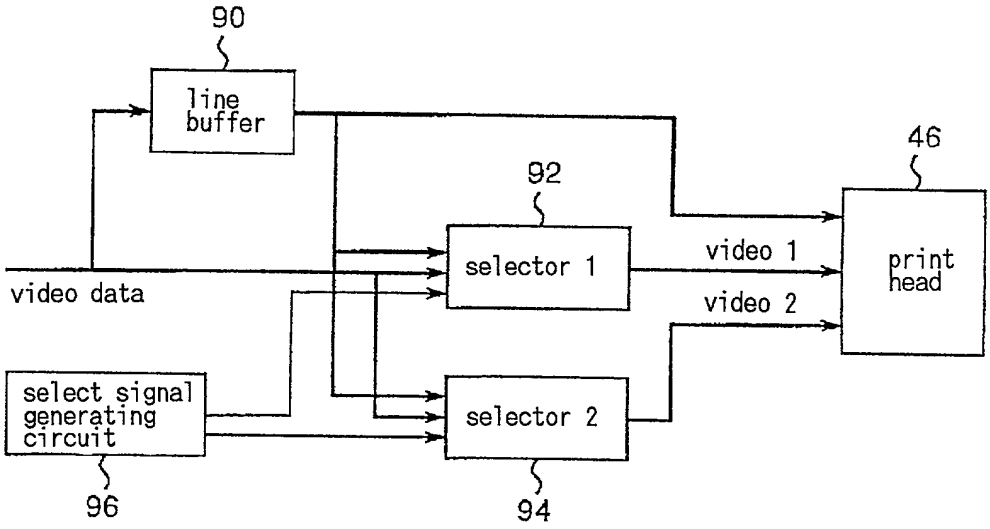

90
line buffer
46
92
selector 1
video 1
print head
video data
video 2
select signal generating circuit
selector 2
96
94

Fig.17

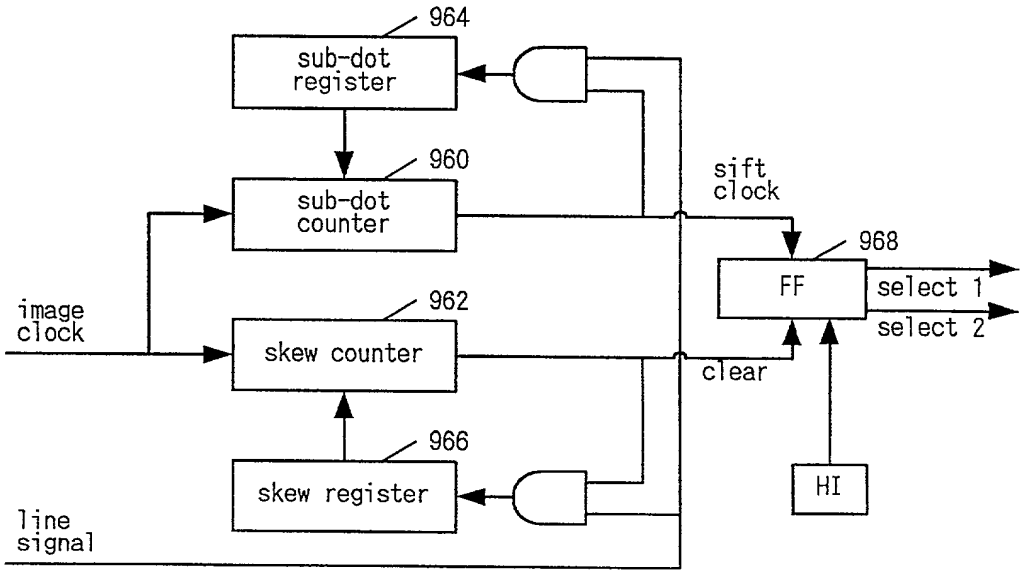

964
sub-dot register
960
sub-dot counter
sift clock
968
FF
select 1
select 2
image clock
962
skew counter
clear
966
skew register
HI
line signal

Fig.18

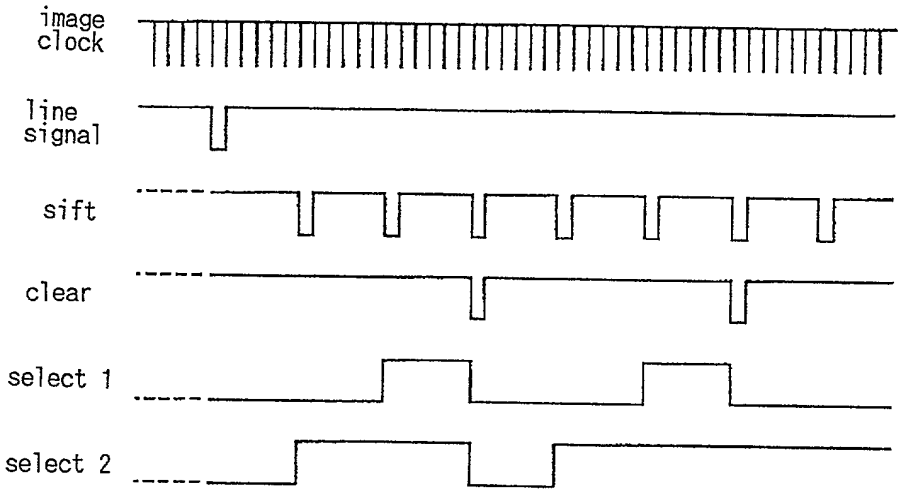


image clock
line signal
sift
clear
select 1
select 2

Fig.19

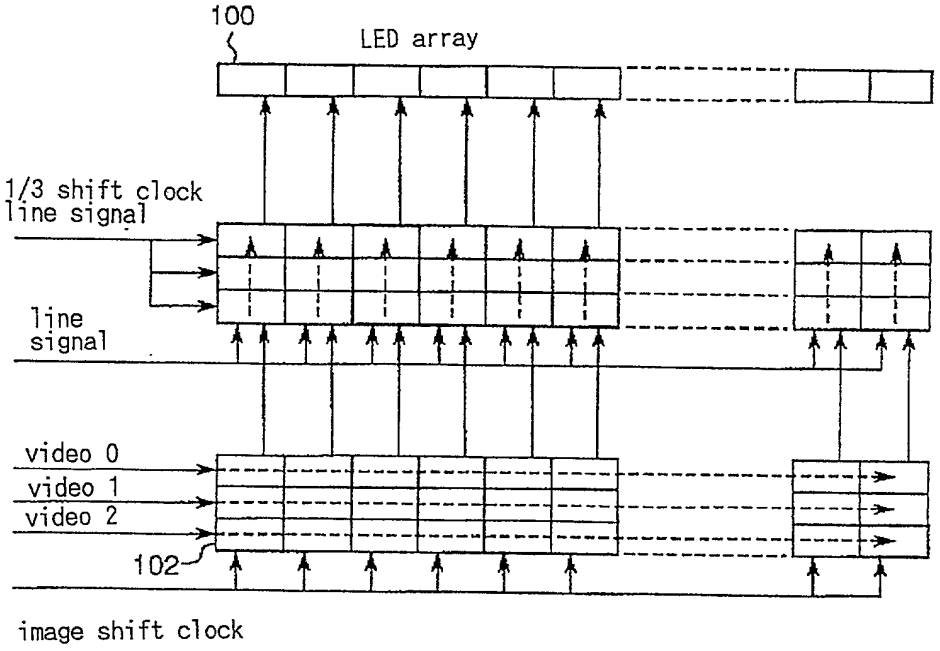
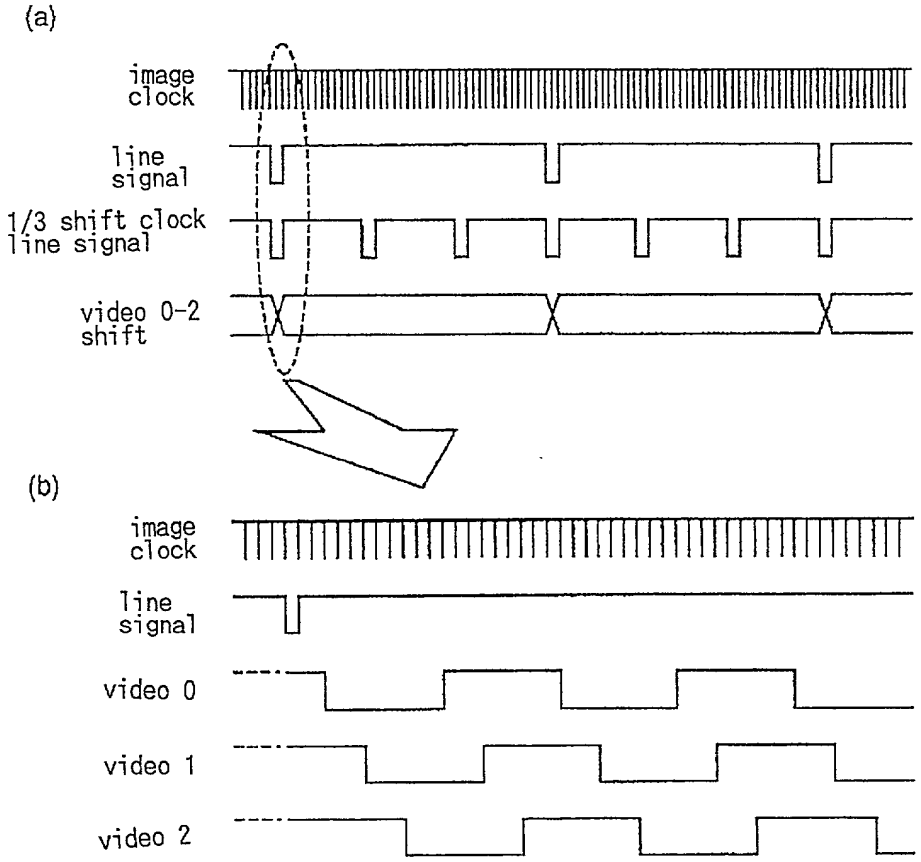

100
LED array
1/3 shift clock
line signal
line signal
video 0
video 1
video 2
102
image shift clock

Fig.20


(a)
image clock
line signal
1/3 shift clock line signal
video 0-2 shift
(b)
image clock
line signal
video 0
video 1
video 2

Attorney Docket No.

COMBINED DECLARATION/POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
DATA PROCESSING APPARATUS, the specification of which

(check one)
- X is attached hereto.
- ___ was filed on _____ as United States Application No.
- ___ PCT International Patent Application Number filed and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
11-258728 (Number)	Japan (Country)	13 / 9 / 1999 (Day/Month/Year Filed)	X Yes ___ No
11-258730 (Number)	Japan (Country)	13 / 9 / 1999 (Day/Month/Year Filed)	X Yes ___ No
11-258732 (Number)	Japan (Country)	13 / 9 / 1999 (Day/Month/Year Filed)	X Yes ___ No
11-258736 (Number)	Japan (Country)	13 / 9 / 1999 (Day/Month/Year Filed)	X Yes ___ No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)
(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)

I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute the patent application identified above and to transact all business in the U.S. Patent and Trademark Office connected therewith: Edward A. Becker, Reg. No. 37,777; Stephen A. Becker, Reg. No. 26,527; Marcel K. Bingham, Reg. No. 42,327; John G. Bisbikis, Reg. No. 37,095; Daniel Bucca, Reg. No. 42,368; Kenneth L. Cage, Reg. No. 26,151; Stephen C. Carlson, Reg. No. 39,929; Tom A. Corrado, Reg. No. 42,439; Paul Devinsky, Reg. No. 28,553; Laura A. Donnelly, Reg. No. 38,435; Margaret M. Duncan, Reg. No. 30,879; Brian E. Ferguson, Reg. No. 36,801; Michael F. Fogarty, Reg. No. 36,139; Willem F. Gadiano, Reg. No. 37,136; Keith E. George, Reg. No. 34,111; John A. Hankins, Reg. No. 32,029; Brian D. Hickman, Reg. No. 35,894; Eric J. Kraus, Reg. No. 36,190; Patrick B. Law, Reg. No. 41,549; Robert E. LeBlanc, Reg. No. 17,219; Jack Q. Lever, Reg. No. 28 ,149; Raphael V. Lupo, Reg. No. 28,363; Christine F. Martin, Reg. No. 39.762; Michael A. Messina, Reg. No. 33,424; Eugene J. Molinelli, Reg. No. 42,901; Christopher J. Palermo, Reg. No. 42,056; Joseph H. Paquin, Jr., Reg. No. 31,647; Robert L. Price, Reg. No. 22,685; Gene Z. Rubinson, Reg. No. 33,351; Joy Ann G. Serauskas, Reg. No. 27,952; David A. Spenard, Reg. No. 37,449; Arthur J. Steiner, Reg. No. 26,106; David L. Stewart, Reg. No. 37,578; Michael D. Switzer, Reg. No. 39,552; Leonid D. Thenor, Reg. No. 39,397; Keith J. Townsend, Reg. No. 40,358; Aaron Weisstuch, Reg. No. P41,557; Edward J. Wise, Reg. No. 34,523; Alexander V. Yampolsky, Reg. No. 36,324; and Robert W. Zelnick, Reg. No. 36,976 all of

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Telephone: 202-756-8000

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor Hirokazu YAMADA

Inventor's signature Hirokazu Yamada Date Sep. 6, 2000
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